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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,206	07/29/2003	Jay Tsao	200312693-1	1124

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EXAMINER	
BAKER, STEPHEN M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,206	TSAO ET AL.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3-6,8-11,14-21,23 and 24* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *2,7,12,13,22 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *072903,022205*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

On page 1, in line 15, "Error codes" apparently should be "Error control codes".

On page 1, in line 17, "codes" apparently should be "control codes".

On page 1 in line 18, "or check bits can" apparently should be "also called check bits, can".

On page 1, in line 19, "error or correction" apparently should be "check".

On page 1, in line 30, "provided" apparently should be "provides".

On page 1, in lines 32-33, "An error correction code (ECC) consists of a group of bits, or codes, associated with a piece of data." apparently should be deleted, as two other terms besides "codes" have already been used by applicant to describe error control code redundancy, and as "codes" is most often used by practitioners synonymously with "codewords".

On page 2, in line 3, "based on" apparently should be "confined within" or the like.

On page 2, in line 7, "faulty" apparently should be deleted.

On page 2, in lines 20-21, "routing a data structure" apparently should be "routing data structure content" or the like.

On page 2, in lines 23-24, "partitioned into separate adjacent bit pair domains, such that a single adjacent bit pair from each memory device is assigned to a given

domain" is unclear and apparently should be "partitioned into domains referred to herein as 'adjacent bit pair domains,' with each adjacent bit pair domain being assigned an adjacent bit pair from each memory device" or the like.

On page 2, in lines 31-32, "routing a data structure" apparently should be "routing data structure content" or the like.

On page 3, in line 4, "Bits" apparently should be "Both bits".

On page 3, in line 6, "aggregated" apparently should be "then aggregated".

On page 4, in line 3, "as a result of" apparently should be "resulting from" or the like.

On page 4, in lines 9-10, "process data structures with more bits than can be detected and corrected by the ECC techniques employed" apparently should be "process data structures having more bits than can be detected and corrected by a single application of the ECC techniques employed" or the like.

On page 4, in lines 11-12, "partitioning a data block and/or data structure into separate domains equal to the number of bits that can be processed by the ECC technique" apparently should be "partitioning the data structure (data block) into domains having a number of bits equal to the number of bits that can be processed by a single application the ECC technique" or the like.

On page 4, in lines 12-15, "Chipkill for the memory system is achieved by populating the separate domains with adjacent bit pairs, such a single adjacent bit pair from each memory device is assigned to a given adjacent bit pair domain" apparently should be "Chipkill for the memory system is facilitated by populating each domain with

adjacent bit pairs such that each domain contains one respective adjacent bit pair from each memory device" or the like, in part as the partitioning further requires a suitable ECC to "achieve" chipkill.

On page 4, in line 17, "achieved" apparently should be "facilitated" or the like.

On page 4, in line 21, "over a data path" apparently should be "over data paths".

On page 4, in line 26, "#K, where K is an integer greater than one" apparently should be "#K".

On page 4, in line 27, "be for example, but not limited to" apparently should be "be, for example but not limited to".

On page 5, in line 2, "width columns" apparently should be "column width".

On page 5, in lines 3-4, "an ECC checker and corrector for a 288 bit data structure would be impractical" apparently should be "an ECC checker and corrector for a 288-bit ECC codeword is considered impractical" or the like.

On page 5, in line 6, "devices" apparently should be "device".

On page 5, in line 9, "sequentially or in parallel" apparently should be "sequentially in less time than otherwise required, or in parallel" or the like.

On page 5, in lines 24-25, "The adjacent bit pair domains are populated with the check bits and data bits from the data block" apparently should be "The check bits for the data block are then added to the adjacent bit pair domains" or the like.

On page 5, in lines 25-26, "The adjacent bit pair domains are assigned adjacent data bit pairs from each memory device" apparently should be "The adjacent bit pair domains are assigned to adjacent data bit pairs for each memory device" or the like.

On page 5, in line 27, "system memory 16" apparently should be "memory devices 18".

On page 6, in line 17, "correctable by the error corrector" apparently should be "correctable within a desired amount of time by the error corrector" or the like.

On page 6, in line 31, "a similar" apparently should be "the same".

On page 6, in line 32, "domain so" apparently should be "domain as needed to cover the memory device width so" or the like.

On page 7, in line 1, "achieved" apparently should be "facilitated" or the like.

On page 7, in line 15, "correction can be performed" apparently should be "correction of more than one ECC codeword can be performed" or the like.

On page 7, line 16, "facilitate speed associated with" apparently should be "facilitate faster" or the like.

On page 7, in line 17, "additional check bit" apparently should be "additional ECC codeword check bit" or the like.

On page 7, line 19, "facilitate speed associated with" apparently should be "facilitate faster" or the like.

On page 7, in line 22, "provides chipkill" apparently should be "facilitates chipkill" or the like.

On page 7, in line 25, "buses larger than the capabilities of ECC techniques" apparently should be "buses larger than the capabilities of a single application of a simple ECC technique" or the like.

On page 8, in line 30, "bit" apparently should be "each bit".

Correction of the remaining errors is left to applicant.

Appropriate correction is required.

Claim Objections

2. Claims 2, 7, 12, 13, 22 and 25 are objected to because of the following informalities:

Regarding claim 2: in line 2, "a same" apparently should be "an".

Regarding claim 7: in lines 1-2, "the plurality of" apparently should be "each of the plurality of".

Regarding claim 12: in line 1, "enable" apparently should be "facilitate" or the like.

Regarding claim 13: in lines 2-4, "store a data structure over the plurality of devices corresponding to a given memory address" apparently should be "store the data structure corresponding to a given memory address in the plurality of devices" or the like.

Regarding claim 22: in line 1, "routing a data structure" apparently should be "routing data structure content" or the like.

Regarding claim 25: in line 1, "the transmitting adjacent bit pair domain data" apparently should be "the adjacent bit pair domain data being transmitted"; in line 3, "path enables chipkill functionality" apparently should be "path to facilitate chipkill functionality" or the like.

Appropriate correction is required.

Conclusion

3. This application is in condition for allowance except for the following formal matters:

Reference is hereby made to the objections noted in the preceding paragraphs.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen M. Baker
Primary Examiner
Art Unit 2133

smb